Fundamentals in MoS_2 Transistors: Dielectric, Scaling and Metal Contacts

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The rise of two-dimensional (2D) crystals has given new challenges and opportunities to the device research. The semiconducting MoS_2 has been considered as a promising ultra-thin body channel for future microelectronic and optoelectronic devices. In this paper, we focus on the fundamental device properties in MoS_2 transistors. In the first part we introduce the dielectric integration on MoS_2 and other 2D crystals by atomic layer deposition, revealing the similarities and differences of dielectric integration on bulk and 2D crystals. Then we discuss scaling of channel length and width of MoS_2 transistors. We also present the different metal contacts on MoS_2, showing Fermi level pinning at metal/2D interfaces. Finally we demonstrate a statistical study on CVD based single layer MoS_2 transistors, therefore to show potentials and limitations on these 2D crystals in device applications.

Introduction

Transition metal dichalcogenides, typically MoS_2, as another typical type of layered structure material, shows good potentials in device application due to a satisfied band gap, thermal stability, carrier mobility, and compatibility to silicon based CMOS process [1-3]. In order to realize high performance MoS_2 MOSFETs, three major issues needs to be completely addressed: how to achieve a low-resistivity metal-semiconductor junction, how to achieve high-quality interface between 2D crystal and dielectric, and device performance at scaled dimensions. As the material cannot be effectively implanted due to the ultrathin nature, the contact resistance (R_c) is mostly determined by the Schottky barrier height (SBH) at the MoS_2/metal interface. This contact resistance at the MoS_2/metal junction is tremendously larger than other contacts at metal/low-dimensional systems like graphene or carbon nanotube due to the enlarged SBH because of the much larger band gap of MoS_2, as expected. Thus to find a metal or alloy which has the work function located near or even into the conduction (valence) band edge for n-type (p-type) transistors without pinning becomes significantly important. Also, for the second issue, although the high-k dielectric has been successfully demonstrated previously [4], the interface between high-k dielectric needs be systematically studied. The third issue is related with transistor dimension, which determines the packing density for a single chip. For potential applications, the performance limitation of MoS_2 transistors associated with channel length/width scaling must be investigated [5,6].

Dielectric Integration on 2D Crystals

Researchers have noticed that the deposition of high-k dielectrics onto 2D crystals, such as graphene, is not as easy as deposition onto bulk crystals. A typical example is the

failure of Al_2O_3 deposition on graphene basal plane with trimethylaluminum (TMA) and water as ALD precursors, which is the most reliable ALD process with a wide process window. This failure has been understood to be caused by the difficulty of forming chemical bonds on the graphene basal plane due to existing global sp^2-hybridation [7,8]. Despite several successful attempts to integrate high-k dielectrics onto 2D systems [9,10], the integration of high-k dielectric onto such 2D crystals has not been thoroughly studied. We focus on the growth of ALD Al_2O_3 on two typical 2D materials: boron nitride, a sister material of graphene and previously used as a graphene dielectric [11]; and MoS_2, a promising layer-structured semiconducting material with a satisfying band gap.

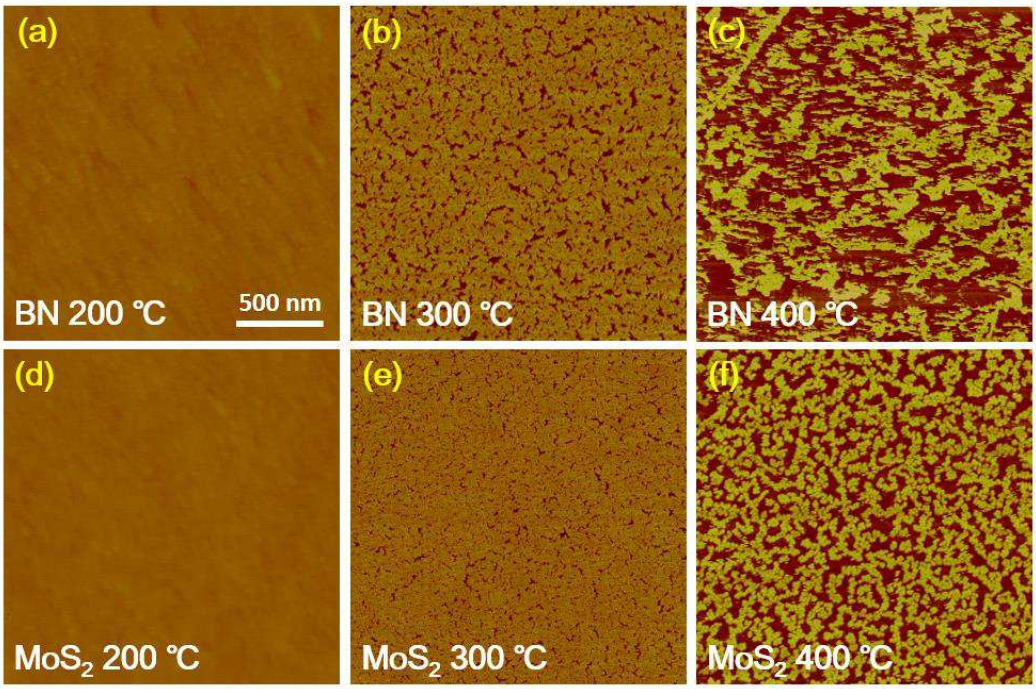

Figure 1: AFM images of BN or MoS_2 surface after 111 cycles of ALD Al_2O_3 at 200ºC, 300℃ and 400℃. All images are taken in a 2 μm by 2 μm region with a scale bar of 500 nm.

Figure 1(a)-1(f) show selected AFM images on BN and MoS_2 surfaces after 111 ALD cycles at 200°C, 300°C and 400°C, with an expected Al_2O_3 thickness of ~10 nm with TMA and water as precursors. The Al_2O_3 growth rate on SiO_2 substrates did not have significant temperature dependence; however, its growth on BN and MoS_2 flakes was strongly temperature dependent. We observed a uniform Al_2O_3 layer formed at 200°C on both BN and MoS_2 substrates. Our previous study showed that the leakage current density was relatively small (~$2x10^{-4}$A/cm^2 under 1 V gate bias) for MoS_2 based metal-oxide-semiconductor structure, suggesting that the ALD Al_2O_3 thin film on MoS_2 was of good quality [2]. With elevated growth temperatures, it was obvious that the Al_2O_3 film was not uniform on both BN and MoS_2 substrates. When the growth temperature was increased to 250°C, pinhole defects started to appear at the 2D surface. With further increase of growth temperatures, these pinholes tended to expand and finally connect with each other, leaving island like Al_2O_3 clusters on the 2D basal plane. In contrast to the growth on basal plane, the growth on edges remain constant at the range between 200°C to 400°C°, due to the existence of dangling bonds at the basal edges.

Channel Length Scaling of MoS_2 Transistors

We fabricated sets of MoS_2 MOSFETs with various channel length. Each set was fabricated on the same rectangular MoS_2 flake, so the scaling effect can be directly observed and compared without needing to correct for geometry and thickness variations. The flakes were mechanically exfoliated from a bulk ingot as described in previous studies and transferred to a heavily doped Si substrate with a 300 nm SiO_2 capping layer. The heavily doped silicon substrate serves as the global back gate and the SiO_2 as the dielectric. Here we select the MoS_2 devices fabricated on a ~5 nm thick crystal which corresponds to ~6 layers with a rectangular shape as representatives.

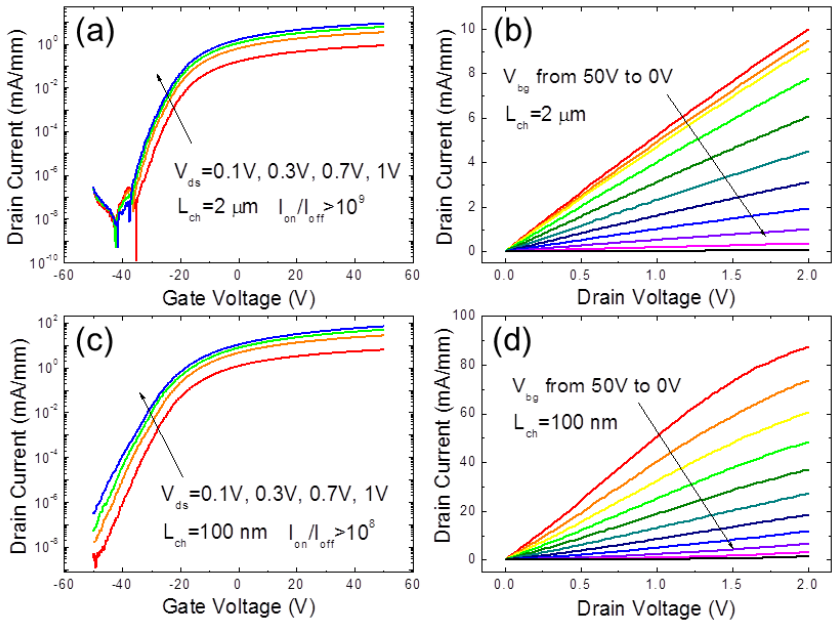

Figure 2: (a) Semi-log plot of the transfer characteristics of a 2 μm long device fabricated on a 5 nm thick MoS_2 crystal. Drain voltage is applied from 0.1 V to 1 V with a 0.3 V step. (b) Output characteristics of the same device. (c)(d) Transfer and output characteristics from a device with L_{ch}=100 nm.

We examined the transistor characteristics of both long-channel and short-channel MoS_2 MOSFETs. The study was carried out on the same sets of devices. Considering that the monolayer has been shown to have a larger bandgap and hence a lower mobility and larger contact resistance, we fabricated the devices on a few-layer crystal for a better tradeoff between the on/off ratio and device performance. Note that the dielectric constant of MoS_2 is only around 3.3, according to a previous theoretical study [12], and a 5 nm thick crystal would be thin enough for short channel devices to turn off completely. Figure 2 shows the transfer and output curves for the 2 μm and 100 nm channel length devices. Drain current saturation was observed in short channel devices as shown in Figure 2(d). Because of their large bandgap of 1.2 eV, these devices, unlike graphene, can be easily turned off. Even though the thickness of gate dielectric is extremely large (300 nm), which results in a much degraded electrostatic control, still no evident short channel effects were observed with channel lengths down to 100 nm. For this short channel device, the on-current is reaching 70 mA/mm at V_{ds}=1 V, and the current on/off ratio is over 10^7 for V_{ds}=1 V, and is able to maintain an on/off ratio of 10^9 at V_{ds}=0.1 V. Benefiting from its ultrathin body, the on/off ratio doesn't drop much compared to the 2

μm long device which has a current on/off ratio up to ~10^{10}, showing good immunity to short channel effects. Note that significant short channel effects could be observed on other planar devices, such as InGaAs or Ge, when the gate length was scaled down to 150 nm. Our observation of transistor behavior without evident short channel effects with 300 nm SiO_2 indicates that the enhancement of electrostatic control by reducing the gate dielectric thickness down to several nanometers would significantly push the scaling of channel length down to sub-10 nm for MoS_2 devices. This is beyond the range of conventional semiconductors. The superior immunity to short channel effects of MoS_2 not only originates from its ultrathin body nature, but is also due to the low dielectric constant of MoS_2 itself.

Channel Width Scaling of MoS_2 Transistors

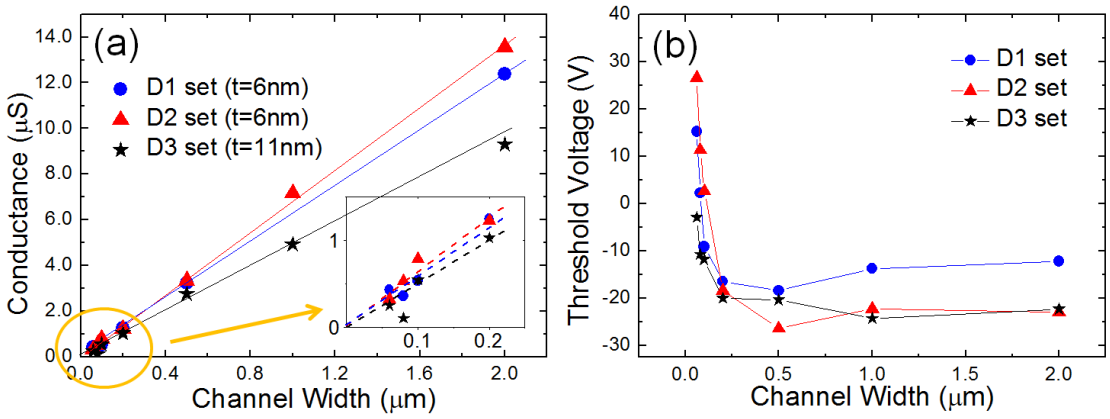

Fig. 3. (a) Extracted channel conductance of all sets of devices versus channel width. (b) Extracted threshold voltage of all sets of devices versus channel width.

We study the channel width scaling associated with The V_T is extracted from the linear extrapolation method at a low drain voltage. Threshold voltages for all three sets of devices are plotted in Figure 3(b). Similar trends can be observed for all sets of devices. The V_T remains constant for transistors with wider channel width (W>500 nm). As the width of the channel is narrowed down to 200 nm, we start to observe the V_T shift to positive values. Apparently, transistors with thinner bodies (D1 and D2) are more likely to be influence by this effect. For one of the 6 nm thick set of transistors (D2), the threshold voltage ultimately shifts from -20V to 30V, indicating a clear transition from being a depletion-mode transistor to being an enhancement-mode operation just by trimming down the channel width. The geometry of these nanoribbon transistors with channel width less than 100 nm has a similar structure to Si FinFETs, if we ignore that the MoS_2 channel is modulated only from the back gate. Similar trends of V_T shift have also been observed in Si FinFETs as well as InGaAs nanowire transistors. This narrow channel effect was ascribed to the lateral expansion of depletion layer due to fringing field effect or quantum confinement in device channels [13]. However, the channel widths are strickly defined in our MoS_2 transistors thus they cannot have a lateral expansion in depletion layer. Also, they are much wider than those of these Si FinFETs and InGaAs nanowire MOSFETs. We believe that our V_T shift is due to edge depletion, similar to what has been observed in majority carrier GaN nanoribbon devices [14]. The edge depletion could be induced by either electric fields or ambient molecules (e.g. H_2O) adsorbed at the MoS_2 surface. Given

our previous surface study of ALD growth on 2D crystals, these polarized molecules can be strongly adsorbed at MoS_2 surface and even persist at 300-400 ºC [4]. As expected, the V_T of the devices fabricated on the thicker crystal (D3) show relatively minor shifts compared to the devices with thinner flakes, as shown in the same figure. The observation of V_T shifts for MoS_2 transistors with width scaling is important. The 2D nature of MoS_2 and other TMD based transistors makes them difficult to engineer the channel through doping. This demonstrated approach, using the width to achieve V_T adjustments on the same starting channel material in order to realize both enhancement-mode and depletion-mode operation, is a simple and favorable method for circuit designs such as to realize an enhancement-mode/depletion-mode based inverter.

Metal Contacts on MoS_2

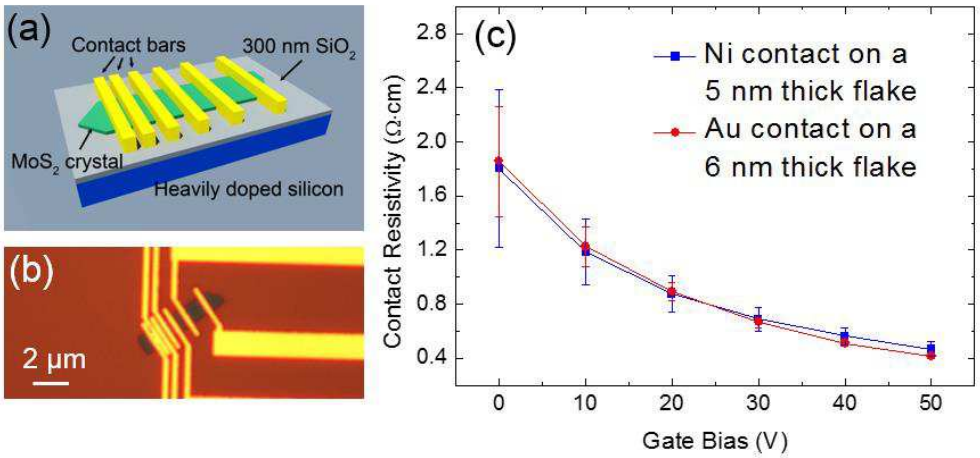

Figure 4: (a) Schematic diagram of the back-gated MoS_2 MOSFETs in a TLM structure. (b) Optical microscope image of one of the fabricated devices. Scale bar is 5 µm. (c) Comparison of contact resistance of Ni/Au on a 5 nm thick device and Au on a 6 nm thick device.

The schematic and corresponding optical microscope image of the devices on a 5 nm thick MoS_2 are shown in Figure 4(a) and 4(b), and have various channel lengths from 2 µm down to 100 nm, as defined by electron beam lithography. Metallization was performed by electron beam evaporation afterwards. The width of the contact bars are 500 nm. To realize high performance short channel devices, one of the major issues is to reduce the source/drain contact resistance. We used Ni/Au as the source/drain metal. No annealing was performed after lift-off process. The Ni/Au contact resistance was extracted using the two-terminal transfer length method (TLM) measurement of the same structure, as shown in Figure 4(c). We extracted the low-field (V_{ds}=50mV) contact resistance from devices with larger channel length (>500 nm), which is much larger than the carrier mean free path in the channel [15], so that the electron transport can be considered as entirely in the diffusive regime. The measurement was performed at room temperature. The contact resistance showed a strong dependence on the back gate bias, as the MoS_2 crystal is electrically-doped under high gate bias, leading to a smaller contact resistance. The smallest R_c measured in the Ni/MoS_2 junction is 4.7±0.5 Ω·mm at 50V back gate bias, and increased to 18.0±5.9 Ω·mm at zero back gate bias. The contact resistance is about a factor of 40 larger than the Pd/graphene contact, for the absence of a

Schottky barrier at metal/graphene junction. Note that the error bars on the left side are significantly larger than those on the right, where the channel is heavily doped. This is attributed to a larger contact resistance on MoS_2 at lower gate bias, leading to a larger absolute error, which is also observed in former graphene TLM study. Generally, the gate dependence of R_c can be attributed to two reasons. One is the existence of a Schottky barrier at the metal/semiconductor interface, as gate bias would change the tunneling efficiency due to band bending at the metal/semiconductor interface. The other is the electrical doping of the semiconductor, as happens with graphene. As a comparison, an Au/MoS_2 TLM structure is also fabricated on another flake with similar thickness (~6 nm), with its contact resistance shown in the same figure. Despite the variance between the two flakes, our results reveal similar contact resistances under the same gate biases. The Schottky barrier between at the MoS_2/Au junction is also observed in a previous temperature dependence study, where the measured mobility showed strong degradation at low temperatures. This could be understood as an increasing contact resistance due to the reduced thermionic emission.

Summary

In this paper, we have studied the fundamental device properties in MoS_2 transistors. We demonstrate the feasibility of ALD dielectric integration on MoS_2 and other 2D crystals and reveal the physical adsorption of precursors. We also study the device scaling properties in MoS_2 transistors. Our results show the superior immunity of MoS_2 transistors to short channel effects and the transition from depletion-mode to enhancement-mode by width scaling. Finally we study the metal contact resistance on MoS_2. We find large contact resistance due to Schottky barrier at the metal/MoS_2 interfaces. The large contact resistance is the major challenge currently in MoS_2 transistor development.

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